Amendments to the Specification:

Please replace the paragraph beginning at page 5, line 24 to line 27, with the following rewritten paragraph:

Fig. 7 is a key to Figs. 7A and 7B, which are a signal-timing diagram for the serializer unit of Fig. 4 and the deserializer unit of Fig. 6 according to one embodiment of the present invention.

Please replace the paragraph beginning at page 9, line 11 to line 15, with the following rewritten paragraph:

Fig. 4 is an example of a serializer unit 400. In this example, system 200 has a core clock signal **CLK** (Figs. 5 and 7A) that clocks core transmit data **CORE_TXD** (Figs. 4, 5 and 7A). In this example, the defined number of data bits is six.

Please replace the paragraph beginning at page 9, line 29 to line 35, with the following rewritten paragraph:

An output line of multiplexer 401 is connected to an input terminal of a first register 403. A clock terminal of register 403 is a connect to a clock line **CLK3x** (Figs. 5 and 7A) that supplies a clock that has a frequency three times (the predefined number of bits divided by two) the frequency of core clock signal **CLK.**

Please replace the paragraph beginning at page 10, line 7 to line 17, with the following rewritten paragraph:

A transmit even data line **td_even** connects the output terminal of register 403 to a first input terminal D1 of a double data rate register 411 in a FPGA I/O buffer 410. Fig. 7A provides a signal trace

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888

for transmit even data line **td_even.** A transmit odd data line **td_odd** connects the output terminal of register 404 to a second input terminal D2 of double data rate register 411. Fig. 7A provides a signal trace for transmit ~~even~~odd data line **td_odd.** The clock terminal of double data rate register 411 is connected to clock line **CLK3x.**

Please replace the paragraph beginning at page 10, line 24 to line 34, with the following rewritten paragraph:

Figs. 5 and 7A include a timing diagram for the double data rate signal on transmit data line **TXDATA** that is connected to one of the serial links between serializer 331 and deserializer 332. In Fig. 5, clock signal **CLK3x** has a frequency three times the frequency of core clock signal **CLK**. Herein, for convenience, the same reference numeral is used for a line and the signal on that line. For serializer unit 400, the data on line **CORE_TXD** are grouped in a set of six lines, e.g., a first set **D0[5:0]**, a second set **D1[5:0]**, a third set **D2[5:0]**, etc.

Please replace the paragraph beginning at page 10, line 35 to Page 11, line 10, with the following rewritten paragraph:

The serial data (Figs. 5 and 7A) on line **TXDATA** is identified by the particular bit in the data set, e.g. D0[0], D0[1], D0[2], etc. Thus, six bits of data from the ASIC block are multiplexed and retimed in the three times the core clock frequency domain. The retimed signals are fed to the double date rate register 411. The frame signal on line **TXFRAME** is sent to the receiver along with the high-speed data from line **TXDATA** for synchronization purposes. The number of serializer units that can be bundled together to

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888

form a serializer is not limited because all the serializer units use the same transmission clock.

Please replace the paragraph beginning at page 11, line 11 to line 21, with the following rewritten paragraph:

Fig. 6 is a more detailed diagram of one embodiment of a deserializer unit, sometimes called a receiver unit, according to one embodiment of the present invention. In this example, deserializer unit 600 receives a received frame signal **RXFRAME** (Fig. 7A) on line **RXFRAME.** (Herein, a signal having a particular reference numeral is carried on a line having the same reference numeral. Accordingly, when a signal is described those of skill in the art understand that that signal is carried on a corresponding line with the same reference numeral.)

Please replace the paragraph beginning at page 11, line 22 to line 26, with the following rewritten paragraph:

Received frame signal **RXFRAME** corresponds to a transmitted frame signal **TXFRAME**. Deserializer unit 600 also receives a data signal **RXDATA** (Fig. 7A) that corresponds to transmitted data signal **TXDATA** that was described above.

Please replace the paragraph beginning at page 11, line 27 to line 36, with the following rewritten paragraph:

A received clock line (not shown) receives a clock signal **RXCLK3x** (Fig. 7A) that is associated with clock signal **CLK3x** that has a frequency three times (the predefined number of bits divided by two) the frequency of core clock signal **CLK** (See Fig. 7A also). In this example, it is assumed that there is no clock skew caused by the traces on the printed circuit board.

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888

Consequently, received clock signal **RXCLK3x** and received data signal **RXDATA** are perfectly lined up at receiver 600.

Please replace the paragraph beginning at page 12, line 1 to line 4, with the following rewritten paragraph:

However, receiver 600 needs to sample the data in the middle of the data "eyes." Accordingly, received clock signal **RXCLK3x** is phase shifted by 90° to create a ninety-degree phase shifted clock **RXCLK3x90** (Fig. 7A).

Please replace the paragraph beginning at page 12, line 12 to line 23, with the following rewritten paragraph:

Received data signal **RXDATA** (Fig. 6) is applied to an input terminal of register 610 and to an input terminal of register 611. A received data odd signal **rd_odd** (Figs. 6 and 7A) from the output terminal of register 611 is applied to an input terminal of an odd retiming register 621. A received data even signal **rd_even** (Figs. 6 and 7A) from the output terminal of register 612 is applied to an input terminal of an even retiming register 622. Ninety-degree phase shifted clock **RXCLK3x90** also is applied to a clock terminal of register 621 and to an inverter on a clock terminal of register 622.

Please replace the paragraph beginning at page 12, line 24 to line 29, with the following rewritten paragraph:

A signal **rd_odd_d** (Figs. 6 and 7B) from the output terminal of register 621 is applied to an input terminal of each of a plurality of six registers 631 to 636. Ninety-degree phase shifted clock **RXCLK3x90**

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888

also is applied to a clock terminal of each of the plurality of registers 631 and 636.

Please replace the paragraph beginning at page 12, line 30 to page 13, line 4, with the following rewritten paragraph:

Each of the plurality of registers 631 to 636 has a clock enable terminal EN. Clock enable terminal EN of register 631 and clock enable terminal EN of register 634 receive a receive buffer enable signal **rxbuf_en_1** (Figs. 6 and 7B). Clock enable terminal EN of register 632 and clock enable terminal EN of register 635 receive a receive buffer enable signal **rxbuf_en_3** (Fig. 6). Clock enable terminal EN of register 633 and clock enable terminal EN of register 636 receive a receive buffer enable signal **rxbuf_en_5** (Fig. 6).

Please replace the paragraph beginning at page 13, line 5 to line 10, with the following rewritten paragraph:

A signal **rd_even_d** (Figs. 6 and 7A) from the output terminal of register 622 is applied to an input terminal of each of a plurality of six registers 641 to 646. Ninety-degree phase shifted clock **RXCLK3x90** also is applied to an inverter on a clock terminal of each of the plurality of registers 641 and 646.

Please replace the paragraph beginning at page 13, line 11 to line 21, with the following rewritten paragraph:

Each of the plurality of registers 641 to 646 has a clock enable terminal EN. Clock enable terminal EN of register 641 and clock enable terminal EN of register 644 receive a receive buffer enable signal **rxbuf_en_0** (Figs. 6 and 7B). Clock enable

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888

terminal EN of register 642 and clock enable terminal EN of register 645 receive a receive buffer enable signal **rxbuf_en_2** (Fig. 6). Clock enable terminal EN of register 643 and clock enable terminal EN of register 646 receive a receive buffer enable signal **rxbuf_en_4** (Fig. 6).

Please replace the paragraph beginning at page 13, line 22 to line 28, with the following rewritten paragraph:

Output signal **rx_buf0_1** (Figs. 6 and 7B) from register 631 is applied to a first input terminal of element 690. Output signal **rx_buf0_3** (Figs. 6 and 7B) from register 632 is applied to a second input terminal of element 690. Output signal **rx_buf0_5** (Figs. 6 and 7B) from register 633 is applied to a third input terminal of element 690.

Please replace the paragraph beginning at page 13, line 35 to page 14, line 5, with the following rewritten paragraph:

Output signal **rx_buf1_1** (Figs. 6 and 7B) from register 634 is applied to a fourth input terminal of element 690. Output signal **rx_buf1_3** (Figs. 6 and 7B) from register 635 is applied to a fifth input terminal of element 690. Output signal **rx_buf1_5** (Figs. 6 and 7B) from register 636 is applied to a sixth input terminal of element 690.

Please replace the paragraph beginning at page 14, line 6 to line 12, with the following rewritten paragraph:

Output signal **rx_buf0_0** (Figs. 6 and 7B) from register 641 is applied to a seventh input terminal of element 690. Output signal **rx_buf0_2** (Figs. 6 and 7B) from register 642 is applied to an eight input terminal

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888

of element 690. Output signal **rx_buf0_4** (Figs. 6 and 7B) from register 643 is applied to a ninth input terminal of element 690

Please replace the paragraph beginning at page 14, line 13 to line 21, with the following rewritten paragraph:

Output signal **rx_buf1_0** (Figs. 6 and 7B) from register 644 is applied to a tenth input terminal of element 690. Output signal **rx_buf1_2** (Figs. 6 and 7B) from register 645 is applied to an eleventh input terminal of element 690. Output signal **rx_buf1_4** (Figs. 6 and 7B) from register 646 is applied to a twelfth input terminal of element 690. Core clock signal **CLK** is applied to a clock terminal of element 690.

Please replace the paragraph beginning at page 14, line 35 to page 15, line 7, with the following rewritten paragraph:

Received frame signal **RXFRAME** (Figs. 6 and 7A) is applied to an input terminal of register 650 and to an input terminal of register 651. A received frame even signal **rframe_even** (Figs. 6 and 7A) from the output terminal of register 651 is applied to an input terminal of a register 661. A received frame odd signal **rframe_odd** (Figs. 6 and 7A) from the output terminal of register 652 is applied to an input terminal of a register 662.

Please replace the paragraph beginning at page 15, line 8 to line 15, with the following rewritten paragraph:

Signal **rx_buf_en_1** (Figs. 6 and 7B) is supplied from the output terminal of register 661 and is applied to an input terminal of a register 663.

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888

Signal **rx_buf_en_3** (Fig. 6) is supplied from the output terminal of register 663 and is applied to an input terminal of a register 665. Signal **rx_buf_en_5** (Fig. 6) is supplied from the output terminal of register 665.

Please replace the paragraph beginning at page 15, line 16 to line 23, with the following rewritten paragraph:

Signal **rx_buf_en_0** (Figs. 6 and 7B) is supplied from the output terminal of register 662 and is applied to an input terminal of a register 664. Signal **rx_buf_en_2** (Fig. 6) is supplied from the output terminal of register 664 and is applied to an input terminal of a register 666. Signal **rx_buf_en_4** (Fig. 6) is supplied from the output terminal of register 665.

Please replace the paragraph beginning at page 15, line 24 to page 16, line 4, with the following rewritten paragraph:

Fig. 7 is a key to Figs 7A and 7B, which are a timing diagram of deserializer unit 600 and serializer unit 400. Ninety-degree phase shifted clock **RXCLK3x90** is used to clock data in received data signal **RXDATA** into double data rate register 610, and to clock data in received frame signal **RXFRAME** into double data rate register 650. Two bits of data, e.g., bits D0[0] and D0[1], are captured per clock, one from a positive edge of ninety-degree phase shifted clock **RXCLK3x90** and one from a negative edge of ninety-degree phase shifted clock **RXCLK3x90.** The two bits of captured data on lines **rd_even** and **rd_odd** are timed using positive and negative edges. The negative edge retimed data is then registered again on the next negative edge of clock **RXCLK3x90,** along with previously positive edge

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888

triggered data. Clock **CLK** is used to demultilplex these two bits onto lines in six lines of data **CORE_RXD.**

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888